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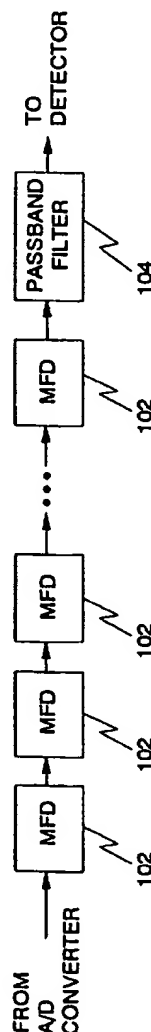
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(54) **Multi-stage digital RF translator.**

(57) An apparatus for performing digital signal frequency translation in a digital receiver is disclosed. The apparatus uses a plurality of mixer-filter-decimator stages (102) for performing the digital signal frequency translation. The translation function converts the digital signal to an intermediate frequency (IF), where such translation is distributed among the plurality of mixer-filter-decimator stages to thereby simplify the mixing requirements.



DIGITAL TRANSLATOR 100

FIG. 1

The present invention relates generally to IF conversion, and more specifically to a multi-stage digital RF translator for performing IF conversion.

Modern communications receivers range from simple FM-stereo radios to more complex, high-bandwidth communications receivers such as those used for satellite communications. These receivers can be implemented using entirely analog technology, or portions of the receiver can be implemented using digital solutions.

The typical analog FM receiver, for example, mixes an incoming FM signal with a variable injection frequency so that the desired channel is positioned at a desired IF (intermediate frequency). This mixing is often termed a frequency conversion or a frequency translation. In more advanced solutions, multiple frequency conversions may be performed to detect the desired frequency. In these advanced receivers, the first conversion is typically performed using a variable injection frequency, while the subsequent conversions use a fixed injection frequency.

With the advent of digital technology, there has been a trend in communications technology to implement a variety of receiver functions using digital circuits. Rapid advances in solid-state and digital-signal-processing technologies have furthered efforts to digitize communications receivers.

One conventional solution implementing digital circuits digitizes the received signal and performs a quadrature mix of the digitized signal to convert it directly to nominally 0 Hz IF. This mixing technique uses digital multipliers that are fed by high speed oscillators to provide sine and cosine injection signals. The mixing is followed by one or more stages of filtering and decimation to isolate the desired receive channel. One or more of the filtering stages may be implemented using simple multiplierless filters for ease of implementation in high speed applications.

A problem with this conventional solution is that the sine and cosine signals injected at the mixer must be generated at very high frequencies (e.g., 88 to 108 MHz for a broadcast FM receiver) to obtain proper conversion results. Generating these signals can be costly and requires a large amount of integrated circuit area.

What is needed is a digital receiver solution that allows digitization and channel isolation in the digital signal processing (DSP) domain of high-frequency receive signals without requiring high-speed DSP oscillators for mixer injection signals, while at the same time using simple high-speed multiplierless filters.

The present invention is a multi-stage digital RF translator for use in a digital receiver. The multi-stage digital RF translator comprises multiple mixer-filter-decimator (MFD) stages. Each stage includes a mixer for performing an IF conversion, a filter for performing a low pass filtering operation to prevent aliasing, and a decimator to resample the data at a lower rate. As

a result, instead of providing a single, complex, high-frequency mixer, the mixing operation is distributed throughout the multiple MFD stages each operating at a different rate. This allows the mixing operation to be simplified, resulting in an easier and less costly implementation.

The first stage is a half-complex mixer. Subsequent stages are implemented using a full complex mixer. Each mixer provides an output signal proportional to the product of the instantaneous values of the complex input signals. The mixer in each stage is implemented such that the injection signal has a frequency that is  $1/4$  the sample rate of the stage. As a result, the injection signals can always be chosen as  $\cos(K\pi/2)$  or  $\sin(K\pi/2)$  where  $K$  is an integer indicating the sample number in time. In other words, the injection signal values can be chosen as a 1, a 0, or a -1. Because the injection signals are limited to these values, multipliers are not needed to implement the mixing function. Instead, the mixing function can be implemented using multiplexing, passing and negation operations.

Once the signal is converted to a lower frequency by the mixer, it is fed into a filter. In a preferred embodiment, the filter is a cascade of simple filter sections that implement a low pass filter. The low pass filter attenuates high frequency components of the signal to prevent aliasing in the decimation stage.

The output of the low pass filter is provided to the decimator where the data is sampled so that one out of  $N$  filter output words is provided as an output signal of the decimator.

In a preferred embodiment, each filter section is a two-tap comb FIR (finite-impulse-response) filter, which is well known in the art.

Distributing the mixing function throughout each MFD stage allows the translator to operate in a manner analogous to successive approximation. The first stage provides a coarse mixing followed by the filtering and decimation functions. Each successive stage brings the signal closer and closer to the desired intermediate frequency (IF) of nominally 0 Hz. Because the mixing is performed in stages, it is less complex than would be required in conventional systems using a single mixer followed by multiple filtering and decimation stages.

The present invention will be described further by way of example, with reference to the accompanying drawings in which:

FIG. 1 is a block diagram illustrating a digital translator according to the present invention implemented using multiple mixer-filter-decimator stages,

FIG. 2 is a block diagram illustrating an example implementation of a mixer-filter-decimator stage, FIG. 3 is a diagram illustrating a half-complex mixer,

FIG. 4 is a block diagram illustrating how a mul-

tplexer could be used with a single mixer-filter-decimator to provide multiple mixer-filter-decimator stages; and,

FIG. 5 is a block diagram illustrating a digital receiver using the digital RF translator according to the present invention.

The present invention is a digital translator circuit that includes multiple mixer-filter-decimator (MFD) stages. As a result, the mixing operation is distributed throughout multiple filter-decimator stages. This is illustrated by the block diagram of FIG. 1. Referring now to FIG. 1, a digital translator 100 is illustrated as including multiple MFD stages 102. Also included is a passband filter 104 as a final stage. Passband filter 104 provides ripple correction.

FIG. 5 is a block diagram illustrating a digital receiver 500. Digital receiver 500 is an example environment in which digital translator 100 according to the present invention can be implemented. Referring now to FIG. 5, an antenna 502 receives a band of input frequencies. Tuning control 504 is used to partially select a desired channel from the band received by antenna 502. An RF amplifier 506 increases the level of the signal from the antenna. Typically, the amount of amplification introduced by RF amplifier 506 is set by the designer, and often automatic gain control is provided. An analog to digital (A/D) converter converts the amplified signal to a digital data stream representing the amplified signal.

Digital translator 100, operating as described below, translates the digital signal to a nominally 0 Hz IF (baseband) for further signal processing. The purpose of such frequency translation is to provide a lower IF frequency, thus facilitating subsequent digital processing. The output of digital translator 100 is fed to a detector 510 which converts the signal to an audio signal. The signal is then provided to audio frequency amplifiers (not shown) and a speaker.

As noted above, digital translator 100 includes multiple MFD stages 102. Each stage includes a mixing, filtering, and decimation function. Because of this unique design, the mixing function is distributed throughout multiple MFD stages 102 and is thereby simplified for ease of implementation.

FIG. 2 illustrates an example implementation of an MFD stage 102. Each MFD stage 102 includes a mixer 202, a filter 222, and a decimator 242. Referring now to FIG. 2, mixer 202 is illustrated as a full-complex mixer. In a preferred embodiment, mixer 202 is actually a half-complex mixer for the first MFD stage 102 and a full-complex mixer for each subsequent MFD stage 102. A half-complex mixer 300 is illustrated in FIG. 3.

A full complex mixer 202 accepts two input signals  $I_n$  and  $Q_n$ .  $I_n$  and  $Q_n$  are a complex pair of signals that together represent a complex signal  $I + jQ$ .  $I_n$  is the in-phase (real part) signal, while  $Q_n$  is the quadrature phase (imaginary part) signal.

The injection signal for full-complex mixer 202 is also a complex signal and can be represented by  $\cos + j\sin$ . Reference character A is the cosine component and Reference character B illustrates the sine component. In other words, the injection signal can be written as  $A + jB$ .

Digital mixer 202 can be thought of as a complex signal multiplier. The instantaneous value of the output of mixer 202 is proportional to the product of the instantaneous values of the two inputs. Mixer 202 is configured as illustrated with multipliers 204 and adders 206 to perform complex multiplication. Full complex multipliers such as the one illustrated in FIG. 2 are well known to persons of skill in the relevant art.

Mixer 202 is implemented such that the injection signal can be chosen with a frequency of  $+f_s/4$ ,  $-f_s/4$ , or 0 where  $f_s$  is the sample rate of the stage. Thus, the values of the injection signals A, B, can always be chosen as 1, 0, or -1. For example, for  $+f_s/4$  the sequence of values for the cosine signal is  $\cos(0) = 1$ ,  $\cos(\pi/2) = 0$ ,  $\cos(\pi) = -1$ , and  $\cos(3\pi/2) = 0$ . As a result, multipliers are not needed to implement mixer 202. Mixer 202 can be implemented using multiplexing, passing and negation operations. These simple operations are much easier to perform at higher speeds than actual multiplication.

For a particular receive channel, in each stage it is determined which of the possible injection frequencies ( $+f_s/4$ ,  $-f_s/4$ , or 0), if chosen, would bring the signal center frequency closest to 0 Hz. For each channel, there is a particular mix of frequencies to pull the signal center frequency closest to 0 Hz. These frequencies can be predetermined and the control for the mixers can be stored in a table for micro-controller execution.

Because the first MFD stage 102 is fed from A/D converter 508, the input signal at the first stage has no imaginary component. Thus, the first stage only requires a half-complex mixer 300 as illustrated in FIG. 3.

An example of mixer 202 is fully discussed in U.S. Patent No. 4,592,074 to Whitehart which is incorporated herein by reference.

The next part in each MFD stage 102 is a filter 222. The purpose of filter 222 is to filter out noise that could be aliased back into the baseband during decimation. In addition, in the first MFD stage 102, filter 222 removes an undesired mixing image from the signal received from mixer 202. In a preferred embodiment, filter 222 stage is a multi-stage comb filter 222. A comb filter 222 is selected because it is one of the easiest and most economical filters to implement.

The filters 222 and mixer 202 for each MFD stage 102 are selected so that the mix places the desired channel passband within the low pass bandwidth of the comb filter 222.

Each comb filter is a FIR filter with M coefficients, all equal to 1. The transfer function of the

comb filter can be expressed as:

Comb filter 222 is followed by an N:1 decimator 242 (2:1 in a preferred embodiment). Decimator 242 samples the data output from comb filter 222 such that the data rate is reduced by a factor of N. Thus, decimator 242 provides data output at a lower rate. The output of decimator 242 is at the lower rate of  $f_s/N$ , where  $N=2$  for a 2:1 decimator.

A single-stage comb filter may not have enough attenuation in the region of interest to prevent aliasing in the decimation stage. To provide the necessary attenuation comb filter 222 can be implemented using multiple, cascaded comb filters 208 as shown in FIG. 2.

Because comb filter 222 can be separated into integration and differentiation, in an alternative embodiment, the differentiation operation can be performed after decimation. Thus, the differentiation can be performed at the lower data rate.

A passband ripple correction filter 104 is implemented to flatten the passband by removing ripple introduced by the filters. In a preferred embodiment, passband filter 104 is an FIR filter.

FIG. 4 illustrates a manner by which two or more of the MFD stages 102 can be implemented using a single, common MFD 404 and a multiplexer 402. According to this implementation, when the circuit is functioning as the first stage of the two or more MFD stages 102, multiplexer 402 is controlled to select input signal A which is the input signal to the first of the two or more stages. When functioning as subsequent stages, multiplexer 402 selects input signal B from the output. In this manner, a single MFD 404 can be used to implement multiple MFD stages 102. Note that because each stage reduces the sample rate by a factor of N, common MFD 404 only needs to execute each stage at a rate not greater than N times the rate of the fastest included stage.

MFD 102 includes storage elements to store intermediate values. MFD 404 is different from MFD stages 102 in that MFD 404 includes additional storage elements to store intermediate values for all stages implemented by MFD 404. Also included in MFD 404 is storage selection circuitry.

Distributing the mixing phase (mixer 202) over multiple MFD stages 102 allows the mixing operation to be simplified. The mixing in multiple stages can be analogized to successive approximation techniques used in analog-to-digital converters, where a first, coarse calculation is performed and then refined in subsequent stages. According to the invention, in the first MFD stage 102, a very coarse mix is performed to allow the signal to be filtered and decimated by a factor of two (2). In other words, the input signal is pulled close enough to the desired IF frequency so the right amount of filtering can be implemented to enable decimation without aliasing. Each subsequent stage continues in this manner until the desired IF of

nominally 0 Hz is reached. Distributing the mixing in this manner lessens the net complexity required for the frequency conversion.

## Claims

1. An apparatus for performing digital signal frequency translation, comprising a plurality of mixer-filter-decimator stages (102), each mixer-filter-decimator stage (102) comprising:
  - mixing means (202) for translating a digital signal to an intermediate frequency signal;
  - filter means (222), connected to said mixing means (202), for low-pass filtering said intermediate frequency signal; and
  - decimation means (242), connected to said filter means (222), for lowering the rate of said filtered intermediate frequency signal.
2. An apparatus as claimed in claim 1, wherein said filter means comprises an integrator and a differentiator.
3. An apparatus as claimed in claim 1, wherein said filter means comprises one or more cascaded comb filters.
4. An apparatus as claimed in claim 1, further comprising a passband filter, connected to said decimation means of a final stage, to provide passband ripple correction.
5. An apparatus as claimed in claim 1, further comprising multiplexing means, coupled to said mixer and to said decimator, for implementing multiple mixer-filter-decimator stages using a single mixing means, filter means and decimation means.
6. A digital receiver, comprising:
  - an antenna configured to receive an RF signal;
  - an RF amplifier, connected to said antenna, configured to amplify said RF signal;
  - an analog-to-digital converter, connected to said RF amplifier, configured to convert said amplified RF signal into a digital signal; and
  - an apparatus as claimed in any one of claims 1 to 5, coupled to said analog to digital converter.
7. A receiver as claimed in claim 6, further comprising a tuner, coupled between said antenna and said RF amplifier, for selecting a carrier frequency from said RF signal;
8. A receiver as claimed in claim 6, further comprising detector means, coupled to said digital trans-

lator, for detecting and amplifying an audio signal  
from said digital translator.

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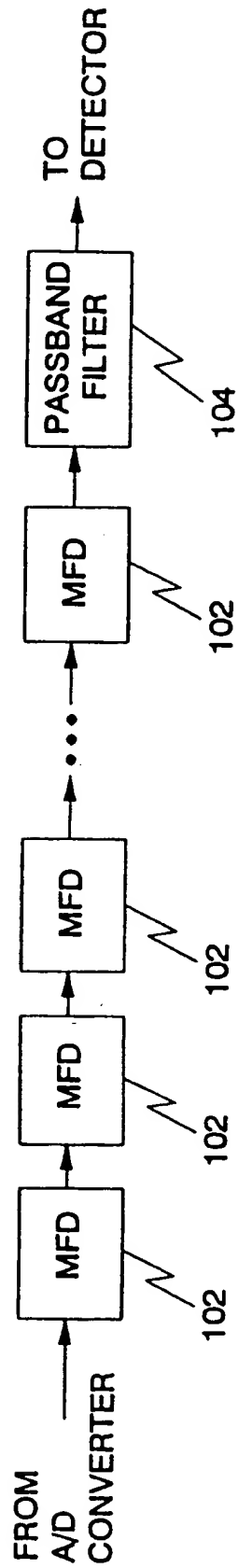
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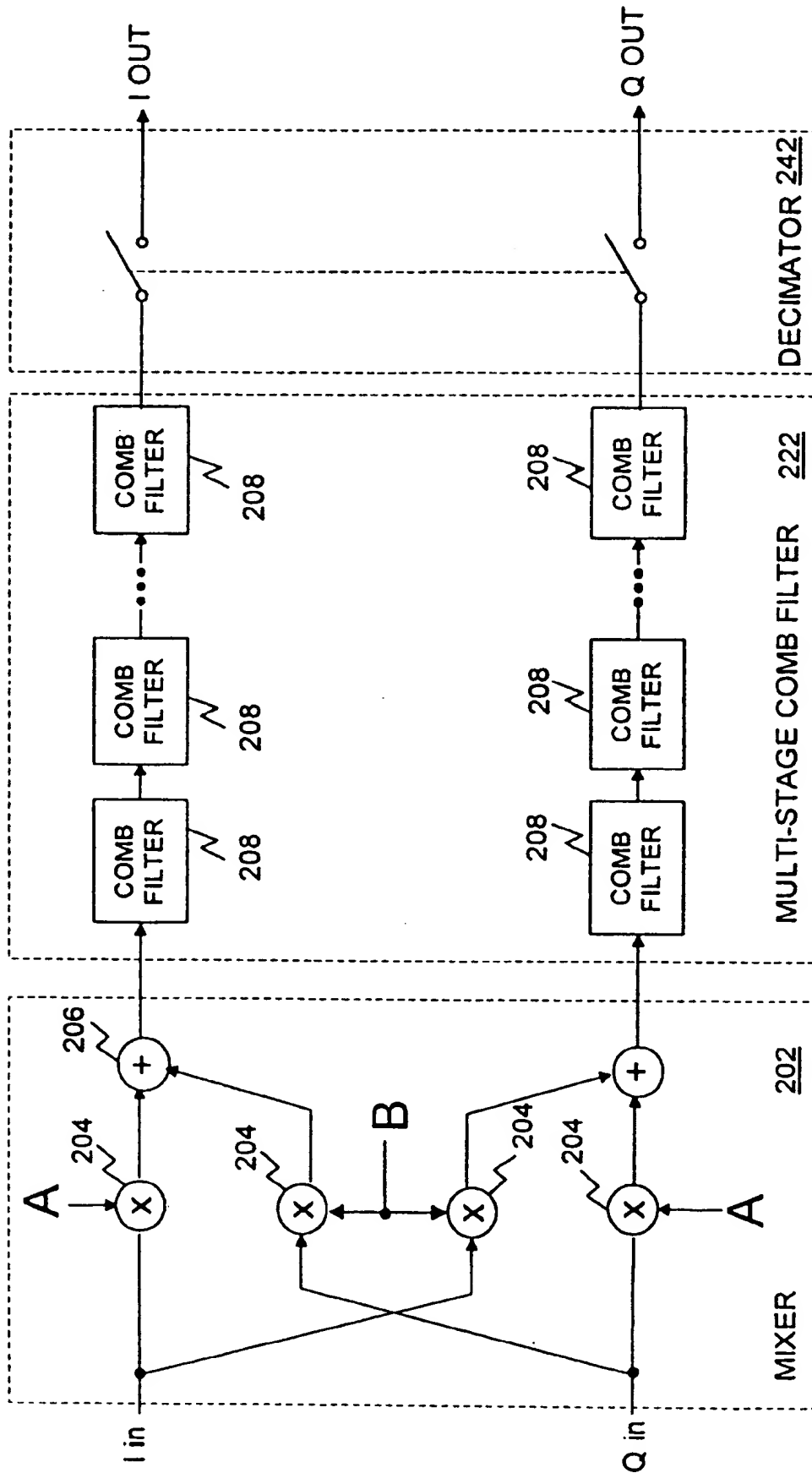
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DIGITAL TRANSLATOR 100

FIG.1



MFD STAGE 102

FIG. 2

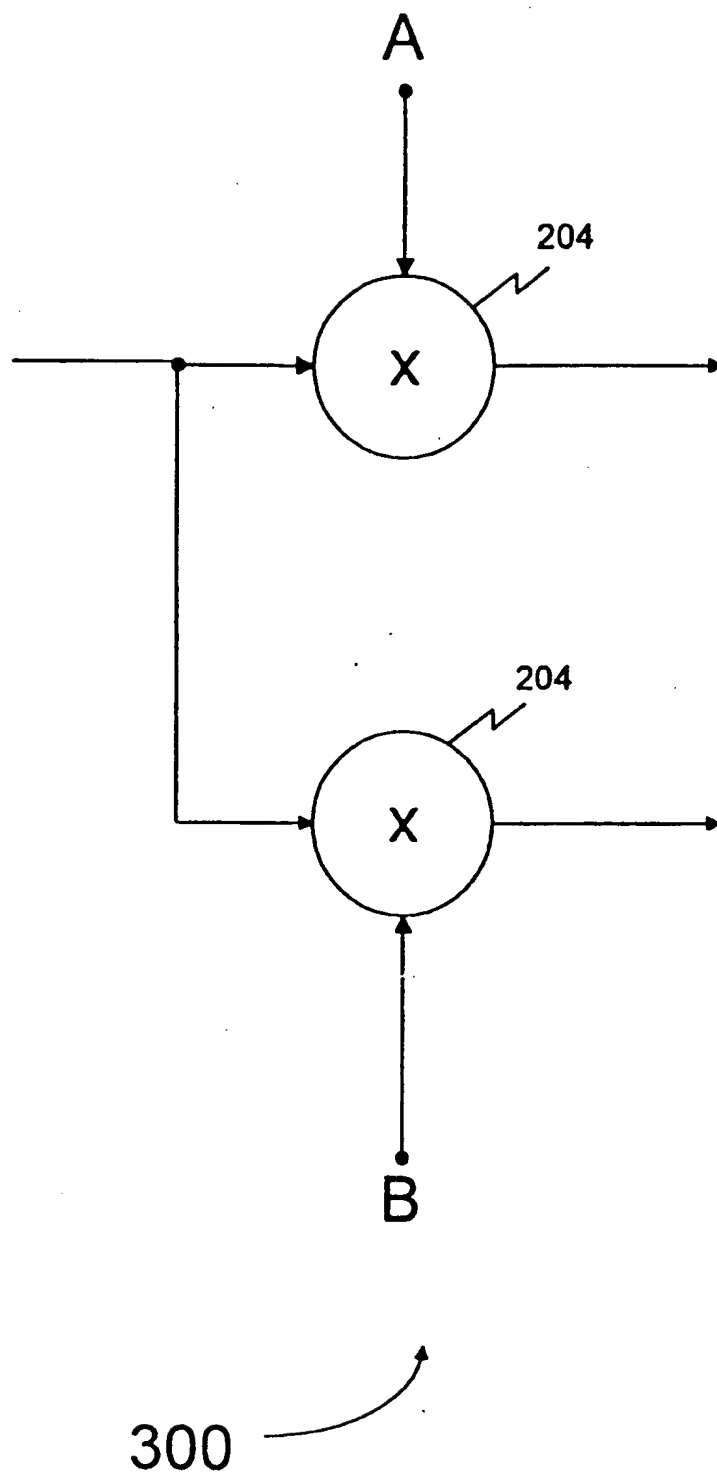


FIG. 3



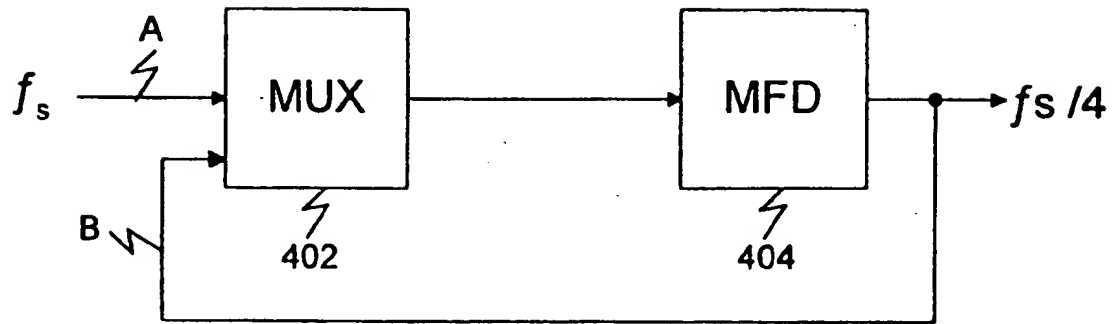


FIG. 4

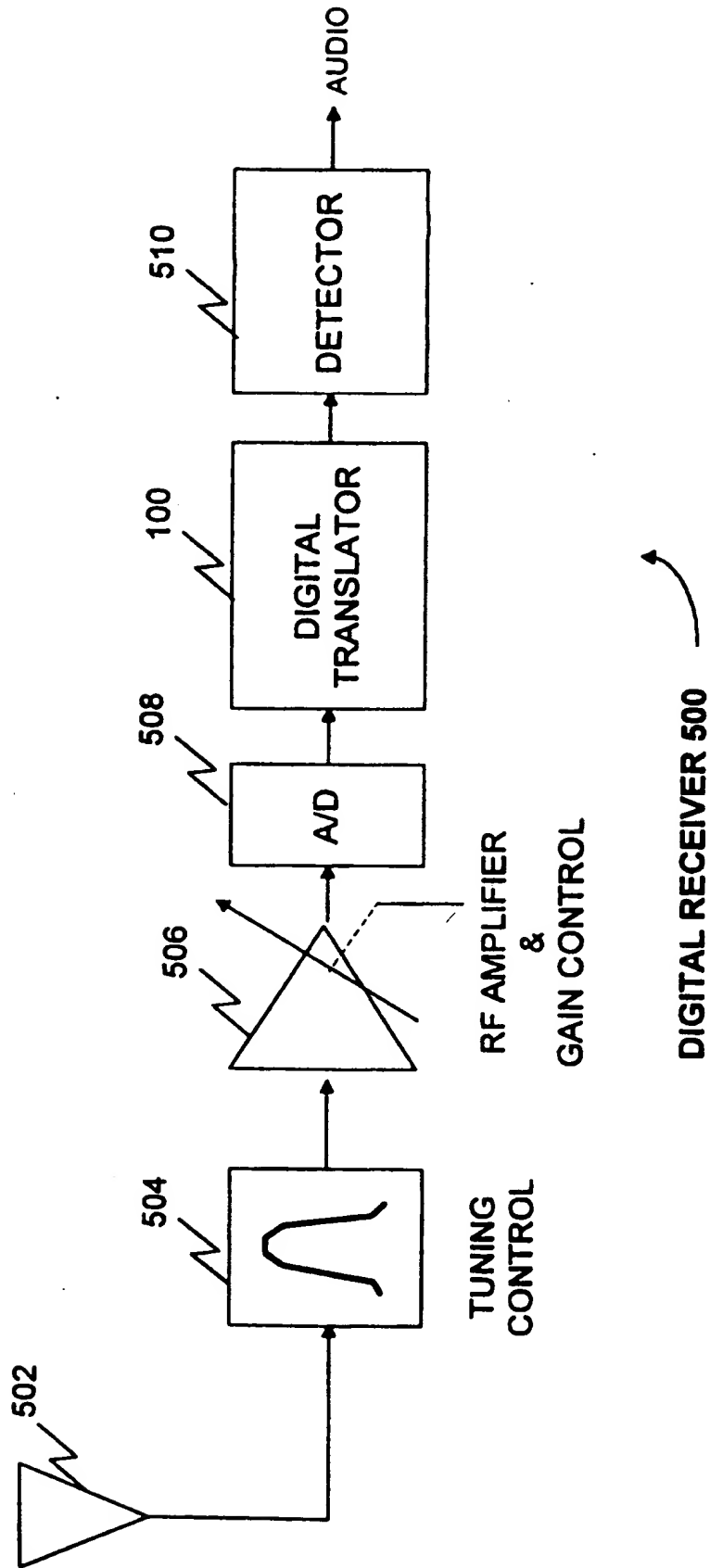


FIG. 5



European Patent  
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# EUROPEAN SEARCH REPORT

Application Number  
EP 94 30 4489

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X	GB-A-2 114 840 (HEWLETT-PACKARD COMPANY)	1-3,5	H03D7/16
Y	* the whole document *	6-8	H03D7/00
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Y	WO-A-86 05936 (MOTOROLA INC)	6-8	
A	* page 15, line 16 - page 27, line 10; figures 4A-16 *	2,3,5	
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A	WO-A-87 07099 (MOTOROLA INC)	1-3,6-8	
	* page 6, line 1 - page 10, line 21; figures 1,3-5 *		
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A	EP-A-0 254 844 (TEKTRONIX INC)	1	
	* abstract; figure 1 *		
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A,D	US-A-4 592 074 (J.W. WHIKEHART)		
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			TECHNICAL FIELDS SEARCHED (Int.Cl.6)
			H03D H04B
The present search report has been drawn up for all claims			
Place of search		Date of completion of the search	Examiner
THE HAGUE		29 September 1994	Dhondt, I
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